UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/538,739	11/09/2005	Yasuhiro Okamoto	029437-0108	7288

22428 7590 11/16/2010

FOLEY AND LARDNER LLP
SUITE 500
3000 K STREET NW
WASHINGTON, DC 20007

EXAMINER	
SALERNO, SARAH KATE	
ART UNIT	PAPER NUMBER
2814	
MAIL DATE	DELIVERY MODE
11/16/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/538,739	OKAMOTO ET AL.	
	Examiner	Art Unit	
	SARAH K. SALERNO	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 September 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-12 and 15-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-11 and 15-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's amendment/arguments filed on 09/21/10 as being acknowledged and entered. By this amendment claims 2, 13 and 14 are canceled, claim 24 has been added claims 1, 3-12 and 15-24 are pending and no claims are withdrawn.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3, 18, 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue (US PGPub 2001/0015446 of record) in view of Shinji (JP Publication 2000-323495).

Claim 1: Inoue teaches a field-effect transistor comprising a Group III nitride semiconductor layer structure including a heterojunction formed by a channel layer made of $In_xGa_{1-x}N$ ($0 \leq x \leq 1$) (603) and an electron supply layer made of $Al_yGa_{1-y}N$ ($0 < y \leq 1$) (604), a source electrode (606) and a drain electrode (608) formed on the semiconductor layer structure while being separated from each other, a gate electrode (607) arranged between said source electrode and said drain electrode, and an insulating film (605a) formed on said Group III nitride semiconductor layer, wherein, said gate electrode has a field plate portion (above 605a) formed on said insulating film while

said field plate portion has a visored shape that overhangs a gate side of said insulating film between said gate electrode and said drain electrode (Fig. 6E; [0061-0067]).

Inoue does not teach the insulating film is a multilayered film that includes a first insulating film and a second insulating film, said first insulating film being made of a compound that includes silicon and nitrogen as constituent elements, said second insulating film having a dielectric constant lower than that of said first insulating film wherein the second insulating film is laminated on said first insulating film. Shinji teaches the insulating film is a multilayered film including a first insulating film (32a) and a second insulating film (32b), said first insulating film being made of a compound that includes silicon and nitrogen as constituent elements, said second insulating film having a dielectric constant lower than that of said first insulating film the second insulating film is laminated on said first insulating film to prevent threshold voltage variation (Fig 1; ABS). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Inoue to have the multilayered film protective film to prevent threshold voltage variation in the device as taught by Shinji (Fig 1; ABS).

Claim 3: Shinji teaches the thickness of said first insulating film is not more than 150 nm (ABS).

Claim 18: Inoue teaches a semiconductor layer structure has a structure in which the channel layer made of $In_xGa_{1-x}N$ ($0 \leq x \leq 1$), the electron supply layer made of $Al_yGa_{1-y}N$ ($0 < y \leq 1$), and a cap layer made of GaN are sequentially laminate [0050]. Inoue does teach these layers are sequentially laminate, however, it is noted that “The

patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made.

Claim 22: Inoue teaches the field plate portion having a visored shape does not overhang any part of said insulating film between said gate electrode and said source electrode (Fig. 6E; [0061-0067]).

Claim 23: Inoue teaches the field plate portion having a visored shape does not overhang any part of said insulating film between said gate electrode and said source electrode (Fig. 6E; [0061-0067]).

4. Claims 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue (US PGPub 2001/0015446 of record) in view of Shinji (JP Publication 2000-323495) and Tan et al. (The Effect of Dielectric Stress on the Electrical characteristics of AlGaN/GaN Heterostructure Field Effect Transistors).

Regarding claim 4, as described above, Inoue and Shinji substantially read on the invention as claimed, except Inoue and Shinji do not teach a dielectric constant of said second insulating film is not more than 3.5. Tan teaches replacing SiN gate dielectric with SiON which has a dielectric constant of less than 3.5 for use in an HFET device. Therefore it would have been obvious to one of ordinary skill in the art at the time the

invention was made to have modified the second insulating film of Inoue and Shinji to not have a dielectric constant more than 3.5 for use in an HFET device as taught by Tan (page 131 2nd paragraph).

5. Claims 5, 6 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue (US PGPub 2001/0015446 of record) and of Shinji (JP Publication 2000-323495), as applied to claim 1 above, and further in view of Mizuta et al. (US Patent 6,483,135 of record).

Regarding claim 15, as described above, Inoue and Shinji substantially read on the invention as claimed, except Inoue and Shinji do not teach the contact layers are arranged between said source electrode and a surface of said semiconductor layer structure and between said drain electrode and a surface of said semiconductor layer structure, respectively. Mizuta teaches the contact layers (3) are arranged between said source electrode (7/8) and a surface of said semiconductor layer (2) structure and between said drain electrode (7/8) and a surface of said semiconductor layer structure, respectively to improve device performance (FIG. 7; Col. 1). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Inoue and Shinji to have the contact layers between the source/drain electrodes and the semiconductor layer to improve device performance as taught by Mizuta (FIG. 7; Col. 1).

Claim 5: Mizuta teaches said insulating film including said multilayered film is formed while being separated from said gate electrode, and said second insulating film

(4a) is provided between said first insulating film (4b) and said gate electrode (5) (FIG. 9e).

Claim 6: Mizuta teaches said second insulating film (4a) is provided between said first insulating film (4b) and said gate electrode (5) and said second insulating film is positioned below said field plate portion (5 above 4a and 4b), and said multilayered film including said first insulating film and said second insulating film is positioned between a drain-side end portion of said field plate portion and said drain electrode (FIG. 9f).

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue (US PGPub 2001/0015446 of record) and Shinji (JP Publication 2000-323495), as applied to claim 1 above, and further in view of Parikh et al. (US PGPub 2003/0020092).

Regarding claim 7, as described above, Inoue and Shinji substantially read on the invention as claimed, except Inoue and Shinji do not teach a third insulating film on said second insulating film, the third insulating film being made of a compound containing silicon and nitrogen as the constituent elements. Parikh teaches adding an additional dielectric layer of SiN on the surface of the existing insulating layers to further protect the device from passivation and impurities that can damage the device during handling [0038]. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Inoue and Shinji to include a third dielectric layer of SiN to further protect the device from

passivation and impurities that can damage the device during handling as taught by Parikh [0038].

7. Claims 8-11, are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue (US PGPub 2001/0015446 of record) in view of Tan et al. (The Effect of Dielectric Stress on the Electrical characteristics of AlGaN/GaN Heterostructure Field Effect Transistors).

Claim 8: Inoue teaches a field-effect transistor comprising a Group III nitride semiconductor layer structure including: a heterojunction formed by a channel layer made of $In_xGa_{1-x}N$ ($0 \leq x \leq 1$) (603) and an electron supply layer made of $Al_yGa_{1-y}N$ ($0 < y \leq 1$) (604), a source electrode (606) and a drain electrode (608) formed on the semiconductor layer structure while being separated from each other, a gate electrode (607) arranged between said source electrode and said drain electrode, and an insulating film (605a) formed on said Group III nitride semiconductor layer, wherein, said gate electrode has a field plate portion (above 605a) formed on said insulating film while said field plate portion has a visored shape that overhangs a gate side of said insulating film between said gate electrode and said drain electrode (Fig. 6E; [0061-0067]).

Inoue does not teach the insulating film is made of a compound that includes silicon, nitrogen and oxygen as constituent elements. Tan teaches a insulating film is made of a compound containing silicon, nitrogen and oxygen as constituent elements as a low stress option for a surface dielectric in an HFET device (page 131 2nd paragraph. Therefore it would have been obvious to one of ordinary skill in the art at

the time the invention was made to have modified the insulating film taught by Inoue to have the constituent elements silicon, nitrogen, and oxygen as a means to lower the stress of the surface dielectric, improving HFET device performance as taught by Tan (page 131 2nd paragraph).

Claim 9: Inoue teaches a field-effect transistor comprising a Group III nitride semiconductor layer structure including: a heterojunction formed by a channel layer made of $In_xGa_{1-x}N$ ($0 \leq x \leq 1$) (603) and an electron supply layer made of $Al_yGa_{1-y}N$ ($0 < y \leq 1$) (604), a source electrode (606) and a drain electrode (608) formed on the semiconductor layer structure while being separated from each other, a gate electrode (607) arranged between said source electrode and said drain electrode, and an insulating film (605a) formed on said Group III nitride semiconductor layer, wherein, said gate electrode has a field plate portion (above 605a) formed on said insulating film while said field plate portion has a visored shape that overhangs a gate side of said insulating film between said gate electrode and said drain electrode (Fig. 6E; [0061-0067]).

Inoue does not teach the insulating film has dielectric constant not more than 3.5. Tan teaches a insulating film that has dielectric constant not more than 3.5 as a low stress option for a surface dielectric in an HFET device (page 131 2nd paragraph. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the insulating film taught by Inoue to dielectric constant not more than 3.5 as a means to lower the stress of the surface dielectric, improving HFET device performance as taught by Tan (page 131 2nd paragraph).

Claim 10: Inoue teaches a field-effect transistor comprising a Group III nitride semiconductor layer structure including: a heterojunction formed by a channel layer made of $In_xGa_{1-x}N$ ($0 \leq x \leq 1$) (603) and an electron supply layer made of $Al_yGa_{1-y}N$ ($0 < y \leq 1$) (604), a source electrode (606) and a drain electrode (608) formed on the semiconductor layer structure while being separated from each other, a gate electrode (607) arranged between said source electrode and said drain electrode, and an insulating film (605a) formed on said Group III nitride semiconductor layer, wherein, said gate electrode has a field plate portion (above 605a) formed on said insulating film while said field plate portion has a visored shape that overhangs a gate side of said insulating film between said gate electrode and said drain electrode and said gate electrode side of said insulating film between said gate electrode and said drain electrode is made of an insulating material (605a) having dielectric constants not more than 4 (Fig. 6E; [0061-0067]).

Inoue does not teach said insulating film is made of an insulating material that includes silicon and nitrogen as constituent elements. Tan teaches a insulating film is made of an insulating material that includes silicon and nitrogen as constituent elements and has dielectric constant not more 4 as a low stress option for a surface dielectric in an HFET device (page 131 2nd paragraph. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the insulating film taught by Inoue to dielectric constant not more than 4 as a means to lower the stress of the surface dielectric, improving HFET device performance as taught by Tan (page 131 2nd paragraph).

Claim 11: Tan teaches the gate electrode side of said insulating film is made of an insulating material containing silicon, nitrogen, and oxygen as the constituent elements (page 131 2nd paragraph).

8. Claims 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue (US PGPub 2001/0015446 of record), Shinji (JP Publication 2000-323495), and Mizuta et al. (US Patent 6,483,135 of record) as applied to claim 15 above, and further in view of Sheppard et a. (US Patent 2001/0017370 of record).

Regarding claim 16, as described above, Inoue, Shinji and Mizuta substantially read on the invention as claimed, except Inoue, Shinji and Mizuta do not teach a contact layer formed by an undoped AlGaN. Sheppard teaches an undoped AlGaN contact layer (17) to improve the characteristics of the device [0011, 0026]. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Inoue, Shinji and Mizuta to make the contact layer out of undoped AlGaN to improve the characteristics of the device as taught by Sheppard [0011, 0026].

Claim 17: Mizuta teaches the field plate portion extends to an upper portion of said contact layer (FIG. 7).

9. Claims 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue (US PGPub 2001/0015446 of record) in view of Shinji (JP Publication 2000-323495), and Hirokawa (US PGPub 2002/0043697 of record).

Claim 19: Claim 1: Inoue teaches a field-effect transistor comprising a Group III nitride semiconductor layer structure including a heterojunction formed by a channel layer made of $In_xGa_{1-x}N$ ($0 \leq x \leq 1$) (603) and an electron supply layer made of $Al_yGa_{1-y}N$ ($0 < y \leq 1$) (604), a source electrode (606) and a drain electrode (608) formed on the semiconductor layer structure while being separated from each other, a gate electrode (607) arranged between said source electrode and said drain electrode, and an insulating film (605a) formed on said Group III nitride semiconductor layer, wherein, said gate electrode has a field plate portion (above 605a) formed on said insulating film while said field plate portion has a visored shape that overhangs a gate side of said insulating film between said gate electrode and said drain electrode (Fig. 6E; [0061-0067]).

Inoue does not teach the insulating film is a multilayered film including a first insulating film and a second insulating film, said first insulating film being made of a compound containing silicon and nitrogen as constituent elements, said second insulating film having a dielectric constant lower than that of said first insulating film. Shinji teaches the insulating film is a multilayered film including a first insulating film (32a) and a second insulating film (32b), said first insulating film being made of a compound containing silicon and nitrogen as constituent elements, said second insulating film having a dielectric constant lower than that of said first insulating film to help form desired shape of the gate electrode due to prevent threshold voltage variation (Fig 1; ABS). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Inoue to have

the multilayered film protective film to prevent threshold voltage variation in the device as taught by Shinji (Fig 1; ABS).

Inoue and Shinji do not teach the size of said field plate is not lower than 0.3μm. Hirokawa teaches a size of said field plate is not lower than 0.3μm to improve device performance (Abs, [0026]). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have specified the field plate length of Inoue and Shinji to be not lower than .3 μm to improve device performance as taught by Hirokawa (Abs, [0026]).

Claim 20: Hirokawa teaches a size of said field plate is not lower than 0.5 μm.

Claim 21: Hirokawa teaches a size of said field plate portion is not more than 70% of a distance between said gate electrode and said drain electrode.

Allowable Subject Matter

10. Claim 12 is allowed. The prior art does not teach the claim 12 limitation of "the drain electrode side is lower than said gate electrode side in a dielectric constant of a capacity formed by said field plate portion, said Group III nitride semiconductor layer, and said insulating film sandwiched therebetween, wherein a part of said insulating film is a multilayered film including a first insulating film and a second insulating film, said first film being made of a compound containing silicon and nitrogen as constituent elements, said second insulating film having a dielectric constant lower than that of said first insulating film, and said gate electrode side is formed by a single layer film of the first insulating film and said drain electrode side is formed by the multilayered film

including said first insulating film and said second insulting film in said insulating film between said field plate portion and a surface of said semiconductor layer structure."

11. Claim 24 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

12. Applicant's arguments filed 09/21/10 have been fully considered but they are not persuasive.

13. Applicant argues that all the claim rejections are traversed based on the combination of Inoue and Shinji.

Applicant's arguments are not persuasive for claims 8-11 because Shinji was not used in combination with Inoue to reject these claims, rather the rejection is based on Inoue in view of Tan.

Applicant argues that Inoue in view of Shinji does not teach claims 1, 3-7, 15-23 because that the protective film of Shinji is provided on a n impurity diffusion layer in order to inhibit impurity diffusion depth variation of an impurity diffusion layer and would serve no purpose in the FET transistor of Inoue. The function of the insulation layer taught by Shinji does not prohibit its ability to replace the insulating layer in Inoue as both are structurally located under a visor shaped field plate portion of a gate electrode in both FET devices as required by the claim limitations.

Conclusion

14. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SARAH K. SALERNO whose telephone number is (571)270-1266. The examiner can normally be reached on M-R 8:00-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Wael M Fahmy/
Supervisory Patent Examiner, Art Unit 2814

/S. K. S./
Examiner, Art Unit 2814